

SPECIFICATION

1 TITLE OF THE INVENTION

DATA PROCESSING APPARATUS HAVING A FLASH
MEMORY BUILT-IN WHICH IS REWRITABLE BY USE
OF EXTERNAL DEVICE

5 CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of
application Serial No. 08/941,254, filed September 30,
1997, which was a continuation of application Serial
No. 08/524,107, filed August 21, 1995, now U. S. Patent
10 No. 5,687,345, which was a continuation of application
Serial No. 08/103,800, filed August 10, 1993, now
abandoned, and which, in turn, was a continuation-in-
part (CIP) of application Serial No. 08/031,877, filed
March 16, 1993, now abandoned, the entire disclosures of
15 which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

The present invention relates to a data
processing apparatus having a built-in electrically
20 rewritable nonvolatile flash memory. Further, the
present invention relates to a technology which makes
the built-in flash memory rewritable by use of an
external device such as a PROM writer in the same way as
a discrete flash memory, and to a technology which is
25 useful when applied to a microcomputer, for example.

1 JP-A-161469 (laid-open on June 26, 1989 and
corresponding to U.S. Application No. 116,607 filed on
November 3, 1987) describes a microcomputer having an
EPROM (Erasable and Programmable Read-Only Memories) or
5 an EEPROM (Electrically Erasable and Programmable
Read-Only Memories) as a programmable nonvolatile memory
formed in a single semiconductor chip. Programs and
data are held in such a nonvolatile memory disposed in
the on-chip arrangement in the microcomputer. Since the
10 EPROM needs ultraviolet rays to erase the stored data,
rewrite cannot be effected unless the chip is removed
from the applied system. Meanwhile, since the EEPROM
can be electrically erased and written, the stored data
can be rewritten with the EEPROM mounted onto the
15 system. However, since memory cells constituting the
EEPROM need select transistors besides the memory
elements, such as MNOSs (Metal Nitride Oxide
Semiconductors), the size of the memory cell becomes
about 2.5 to 5 times as large as that of the memory cell
20 of the EPROM. Therefore, a relatively large area of the
chip is necessary for the nonvolatile flash memory
portion.

JP-A-2-289997 (laid-open on November 29, 1990)
describes a simultaneous erase type EEPROM. This
25 simultaneous erase type EEPROM is synonymous to the
flash memory disclosed in this specification. Data of
the flash memory can be rewritten by implementing a

1 sequence of electrical erase and write operations, and
the memory cell of this flash memory can be constituted
by one transistor in the same way as the EPROM.
Further, the flash memory has the function of
5 simultaneously, electrically erasing all the memory
cells as a bulk or, alternatively, one or more blocks of
memory cells. Therefore, the stored data of the flash
memory can be rewritten with the flash memory kept
mounted on the system (in the on-board state). This
10 simultaneous erase function can shorten the rewrite
time, and also contributes to the reduction of the chip
occupying area.

U.S. Patent 4,701,886 issued on October 20,
1987 to Y. Sakakibara et al discloses a one-chip
15 microcomputer having an EPROM. Data stored in that
EPROM can be changed by externally supplying new data
thereto from an EPROM writer.

U.S. Patent 4,807,114 issued on February 21,
1989 to S. Itoh discloses a microcomputer which is
20 programmable either externally or by its internal
control function.

SUMMARY OF THE INVENTION

The present inventors have made
25 investigations of a microcomputer having a flash
memory mounted thereon. Though the microcomputer
having a built-in flash memory can perform on-board

1 rewrite (namely, rewrite in a state in which the
memory is mounted on a board), for an initial writing,
write efficiency may be, in some cases, higher with a
write device such as a PROM writer before the memory
5 is mounted on a board, that is, before the memory is
mounted onto a system (e.g., an automobile engine
control system, a camera, a VTR, etc.) than with the
on-board write technique, depending on a mode of use
by a user. Thus, the present inventors have first
10 found out the necessity for supporting the write
function by a writer which is versatily utilized
for write operations of both EPROMs and EEPROMs,
such as a PROM writer, by connecting the writer
through a socket adapter, to such a microcomputer
15 with the built-in flash memory, too. Rewrite,
namely, erase and write of the flash memory in this
case requires more complicated control in comparison
with the EPROMs and EEPROMs. To avoid over-erase (a
phenomenon in which a threshold voltage of a memory
20 cell transistor becomes so small and further becomes
negative that normal readout is no longer possible)
which is the problem inherent in the flash memory,
particularly in the case of an erase operation, an
erase technique which effects a pre-write operation
25 for making the write level uniform before commencing
with the erase operation or technique which gradually

1 carries out an erase operation while effecting a verify
function, becomes necessary. A control procedure for
such a processing cannot be assigned to a versatile PROM
writer as such, because a problem occurs in the
5 processing, and it is not practical, either, to cope
with this problem with a writer for exclusive use for
the microcomputer having the built-in flash memory, such
as the PROM writer.

10 It is an object of the present invention to
provide a data processing apparatus having a built-in
flash memory which is user-friendly in writing data
therein by use of an external device such as a PROM
writer, before the apparatus is mounted on a circuit
board.

15 It is another object of the present invention
to provide a data processing apparatus having a function
of rewriting a built-in flash memory by use of an
external device versatily utilized such as a PROM
writer.

20 Further, it is another object of the present
invention to provide a data processing apparatus, which
minimizes the increase of a circuit scale to be
additionally incorporated at this time for the purpose
of data write by the external device.

25 The above and other objects and novel features
of the present invention will become more apparent from
the following description of the specification and the
drawings.

1 Main aspects of the present invention will be explained briefly as follows.

(a) According to one aspect of the present invention, a data processing apparatus includes a
5 central processing unit and an electrically rewritable nonvolatile flash memory both formed in a single semiconductor substrate, and is operable in an operation mode in which the built-in flash memory is rewritable in accordance with commands from an external
10 device, and comprises command latch means which is writable from outside in the above-mentioned operation mode, command analysis (e.g., decoding) means for analyzing (e.g., decoding) predetermined commands latched in the command latch means, and control means for executing sequence control
15 for a rewriting of the flash memory in accordance with a result of the analysis.

(b) During the rewrite operation of the flash memory by the external device, the built-in central processing unit (the central processing unit constituting the data processing apparatus) need not
20 execute separate processing, and may be substantially at halt. In this instance, if the built-in central processing unit is used for executing the processings of the command analysis means and the
25 control means described above, an exclusive circuit for rewriting such as the command analysis means and the control means can be reduced.

1 The external device versatilely utilized, such
as an EPROM writer, has a function of applying a high
voltage for rewrite to a nonvolatile memory device and a
function of supplying an address for rewrite and data to
5 a semiconductor device (LSI) coupled thereto and
including the flash memory in accordance with a write
signal and others. Such an external device supplies
commands, data and addresses asynchronously with respect
to the central processing unit built-in in the data
10 processing apparatus. Thus, the data processing
apparatus may further include, in the structure
described in (a) above, flag means for indicating that a
command is written in the command latch means, data
latch means which is writable from outside when the
15 flag means indicates a command latch state, and address
latch means in which address data is writable from
outside so as to prevent collision between a command and
a data, that are written from the external device in
mutually different cycles, on the latch means. Thereby,
20 the central processing unit reads the command in the
command latch means on the basis of the command latch
state of the flag means.

(c) If the control for the flag means is also
assigned to the central processing unit, the central
25 processing unit must always monitor the content of the
command latch means using a bus cycle, which will be a
wasteful operation. Accordingly, the data processing
apparatus may further include, in the structure

1 described in (b) above, a command decoder for decoding
the latch content of the command latch means and setting
the flag means for the command latch state when decoding
a predetermined command. Thereby, speed-up of control
5 of the flag means will be possible.

(d) If the central processing unit analyzes all
the latched commands, the operation designated by some
of the commands may be too late in timing. An example
is a read command for reading out data from the flash
10 memory. To cope with this problem, the data processing
apparatus may further include, in the structure described
in (c) above, gate means which is provided in an internal
bus and is capable of selecting the operation state where
the command latch means, the data latch means and the
15 address latch means are connected to the flash memory
and to the central processing unit and another operation
state where the command latch means, the data latch means
and the address latch means are connected to the flash
memory but are not connected to the central processing
20 unit, and this gate means being controlled by a signal
generated by the command decoder when it decodes a
command other than the predetermined commands. Under
the condition where such a gate means is open, direct
read access can be made to the flash memory outside the
25 data processing apparatus. The read command may be the
command other than the predetermined commands described
above. With this structure, the flash memory built-in
in the data processing apparatus is equivalent, as

1 seen from the external device such as a PROM writer, to
a discrete flash memory (LSI device) in respect of
rewrite and read operations.

(e) A procedure control program for rewriting the
5 flash memory, which the central processing unit should
execute, is stored in advance in the flash memory, and
this program is transferred to a RAM in the data
processing apparatus in response to setting of the
rewrite operation mode by the external device. The
10 program transferred to the RAM can be executed by the
central processing unit.

(f) The quantity of the data to be stored in the
flash memory is different depending on the usage of the
data or on the kind of the data such as a program, a
15 data table, control data, etc. When this fact is taken
into consideration, it is better to allocate a plurality
of kinds of memory blocks having mutually different
memory capacities, as a simultaneously erasable unit in
the flash memory, in order to eliminate wasteful write
20 operations caused by simultaneous erasure of all memory
blocks of the built-in flash memory for local or partial
rewrite of the data held by the built-in flash memory
after the data processing apparatus having the flash
memory has been mounted onto the system (circuit board)
25 to thereby improve rewrite efficiency.

According to the above-described structures,
since the rewrite sequence is accomplished by built-in
circuits of the data processing apparatus having the

1 built-in flash memory, in accordance with commands given
asynchronously from the external device, the external
device has only to apply the commands to the data
processing apparatus before it gives the apparatus data
5 and address data, in the same way as it gives the data.
And, data write in the built-in flash memory of the data pro-
cessing apparatus can be effected by coupling (electrically
connecting) the flash memory with the external device versa-
tilely used such as a PROM writer, through a socket adapter.

10 The built-in central processing unit of
the data processing apparatus controls the rewrite
sequence designated by the commands, eliminates the
necessity of exclusive circuits for the rewrite sequence
control or reduces the number of such circuits, and
15 accomplishes the reduction of the chip area of the data
processing apparatus. Further, the control sequence for
rewrite can be changed by modifying software that are
to be executed by the central processing unit, and this
makes it possible to set conditions such as a write time
20 in a manner which matches with characteristics of the
memory devices that constitute the flash memory.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B are diagrams for explaining a
structure and the principle of operation of a flash
25 memory.

Fig. 2 is an explanatory view showing the
structural principle of the flash memory for a memory

1 cell array.

Fig. 3 is an exemplary block circuit diagram of a flash memory in which the memory capacity of simultaneously erasable memory blocks is made mutually
5 different.

Fig. 4 is a functional block diagram of a microcomputer having a built-in flash memory according to a first embodiment, in which a rewrite processing of the built-in flash memory is executed by a PROM writer.

10 Fig. 5 is a functional block diagram of a microcomputer having a built-in flash memory according to a second embodiment, in which a rewrite processing of the built-in flash memory is executed by a PROM writer.

Figs. 6A to 6C are timing charts showing an
15 example of command write by a PROM writer.

Fig. 7 is a timing chart showing an example of a data write cycle for a flash memory by CPU control.

Fig. 8 is a block diagram showing details of a structure of a microcomputer corresponding to the
20 microcomputer shown in Fig. 5.

Fig. 9 is a plan view showing the microcomputer shown in Fig. 8 in a packaged state.

Fig. 10 is an overall block diagram of the flash memory built-in in the microcomputer shown in
25 Fig. 8.

Fig. 11 is an explanatory view showing an example of the mode of division of a memory block.

Figs. 12A to 12C are explanatory views showing

1 examples of a control register and an erase block
designation register.

Fig. 13 is a block diagram showing details of
hardware to cope with a PROM writer rewrite mode by a
5 command system in the microcomputer shown in Fig. 8.

Fig. 14 is an explanatory view showing a
control form of a command flag, a data flag and bus
switches.

Figs. 15A and 15B show an exemplary detailed
10 flowchart of a flash memory write control procedure with
the microcomputer in an on-board state.

Figs. 16A and 16B show an exemplary detailed
flowchart of a flash memory erase control procedure with
the computer in an on-board state.

15 Fig. 17 is an explanatory view showing
altogether states of flags CF and DF during the write
operation by the PROM writer and the operation of a CPU.

Fig. 18 is an explanatory view showing
altogether states of the flags at the time of write
20 verify by the PROM writer and the operation of the CPU.

Figs. 19A and 19B are explanatory views
showing altogether states of the flags at the time of
reset by the PROM writer and the operation of the CPU.

Figs. 20A and 20B show an exemplary flowchart
25 of the operation of the PROM writer at the time of data
write by the command system.

1 Figs. 21A and 21B show an exemplary flowchart
of the operation of the PROM writer at the time of erase
by the command system.

Fig. 22 is a main flowchart showing the
5 processing of the CPU for the command given from the
PROM writer.

Figs. 23A and 23B are flowcharts showing
processing routine of Erase and a processing routine of
Erase Verify shown in Fig. 22.

10 Fig. 24 is a flowchart showing a processing
routine of Auto Erase shown in Fig. 22.

Figs. 25A and 25B are flowcharts showing a
processing routine of Program and a processing routine
of Program Verify shown in Fig. 22.

15 DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments of the present invention will be
described in the order of the items listed below.

- [1] Principle of operation of a flash memory
- [2] Division into a plurality of memory blocks having
20 mutually different storage capacities
- [3] Principle of command system data write in a flash
memory by PROM writer
- [4] Microcomputer
- [5] Built-in flash memory
- 25 [6] Hardware adapted to command system
- [7] Command specification of data write and others in
a flash memory by PROM writer

- 1 [8] Data write in a flash memory in on-board state
[9] Data write operation by command system
[10] Operation of PROM writer for data write by
command system
5 [11] Operation of CPU for data write by command system
[12] Compatibility between a flash memory built-in in
a data processing apparatus and a discrete flash
memory LSI in terms of write specification, as
seen from PROM writer

- 10 [1] Principle of operation of a flash memory

Figs. 1A and 1B illustrate a structure and the principle of operation of a flash memory. A memory cell typically depicted in Fig. 1A comprises an insulated gate field effect transistor having a two-layered gate structure. In the drawing, reference numeral 1 denotes a P type silicon substrate, reference numeral 2 denotes a P type semiconductor region formed in the silicon substrate 1, and reference numerals 3 and 4 denote N type semiconductor regions. Reference numeral 5 denotes a floating gate formed on the P silicon substrate 1 through a thin oxide film 6 (10 nm-thick, for example) as a tunnel insulating film, and reference numeral 7 denotes a control gate formed on the floating gate 5 through the oxide film 8. A source is constituted by region 4 and a drain by region 3. Data stored in this memory cell is held substantially as a change of

1 a threshold voltage by a transistor. Hereinafter, the
description will be given on the case where the
transistor for storing data (hereinafter also referred
to as the "memory cell transistor") in the memory cell
5 is of the N channel type unless specifically described
otherwise.

The data write operation in the memory cell is
accomplished, for example, by applying a high voltage to
the control gate 7 and the drain and injecting electrons
10 from the drain side to the floating gate by avalanche
injection. Due to this write operation, the threshold
voltage of the memory transistor, as viewed from its
control gate 7, becomes higher than that of the memory
transistor under an erase state, to which the write
15 operation is not executed, as shown in Fig. 1B.

On the other hand, the erase operation is
accomplished, for example, by applying a high voltage to
the source and extracting the electrons from the
floating gate 5 to the source side by the tunnel
20 phenomenon. Due to this erase operation, the threshold
voltage of the memory transistor as viewed from its
control gate 7 is lowered as shown in Fig. 1B. In Fig.
1B, the threshold value of the memory cell transistor is
set for a positive voltage level in both of the write
25 and erase states. In other words, the threshold voltage
under the write state is set to be higher than the word
line selection level applied from a word line to the
control gate 7 and the threshold voltage under the erase

1 state is set to be lower. Since both of the threshold
voltages and the word line selection level have such a
relationship, the memory cell can be constituted by one
transistor without using a select transistor in
5 combination. To electrically erase the stored data, the
electrons accumulated in the floating gate 5 are
extracted to the source electrode. Since erase of the
stored data is thus effected, a greater quantity of
electrons than the quantity of the electrons injected
10 into the floating gate 5 during the write operation are
extracted if the erase operation is continued for a
relatively long time. Accordingly, if over-erase is
carried out such as when the electrical erase is
continued for a relatively long time, the threshold
15 voltage of the memory cell transistor changes to a
negative level, for example, and there occurs the
problem that the memory cell transistor is selected at a
non-selection level of the word line, too.
Incidentally, the write operation can be effected also
20 by utilizing the tunnel current in the same way as the
erase operation.

In the read operation, the voltages applied to
the drain 3 and to the control gate 7 are limited to
relatively low values so that a weak write is not made
25 in the memory cell or in other words, undesired
injection of carriers is not made in the floating gate
5. For example, a low voltage of above 1 V is applied
to the drain and a low voltage of about 5 V is applied

1 to the control gate 7. The logic values "0" and "1" of
the data stored in the memory cell can be discriminated
by detecting the magnitude of the channel current
flowing through the memory cell due to these applied
5 voltages.

Fig. 2 shows the structural principle of a
memory cell array using the memory cell transistors
described above. This drawing, for purposes of the
present discussion, illustrates a matrix arrangement of
10 only four memory cell transistors Q1 to Q4. Among the
memory cells arranged in matrix in X and Y directions,
the control gates (selection gates of the memory cells)
of the memory cell transistors Q1, Q2, (Q3, Q4) arranged
on the same row are connected to a corresponding word
15 line WL1 (WL2) and the drain regions (input/output nodes
of the memory cells) of the memory cell transistors
Q1, Q3 (Q2, Q4) disposed on the same column are
connected to a corresponding data line DL1 (DL2). The
source regions of the memory cell transistors Q1, Q3
20 (Q2, Q4) are connected to a source line SL1 (SL2).

Table 1 shows an example of voltage conditions
for the erase and write operations for the memory cells.

Table 1

OPERATION MODE	MEMORY CELL	SELECT/NON-SELECT	SOURCE	DRAIN	GATE
WRITE	Q1	SELECT	0 V	6 V	12 V
	Q2	NON-SELECT	0 V	0 V	12 V
	Q3	NON-SELECT	0 V	6 V	0 V
	Q4	NON-SELECT	0 V	0 V	0 V
ERASE (1)	Q1, Q3	SELECT	12 V	0 V	0 V
	Q2, Q4	NON-SELECT	0 V	0 V	0V
ERASE (2)	Q1, Q2	SELECT	5 V	0 V	-10 V
	Q3, Q4	NON-SELECT	5 V	0 V	0 V

ERASE (1): POSITIVE VOLTAGE SYSTEM ERASE OPERATION

ERASE (2): NEGATIVE VOLTAGE SYSTEM ERASE OPERATION

1 In Table 1, the term "memory cell" means a memory cell transistor and the term "gate" means the "control gate" of the memory cell transistor as the selection gate. In Table 1, the erase operation by a
 5 negative voltage system is accomplished by applying a negative voltage of -10 V, for example, so as to generate a high electric field necessary for erase. As can be understood clearly from Table 1, simultaneous erase can be made in the erase operation of a positive
 10 voltage system for those memory cells at least the sources of which are connected in common. According to the structure shown in Fig. 2, therefore, the four memory cells Q1 to Q4 can be simultaneously erased if the source lines SL1 and SL2 are connected. In this

1 case, the size of the memory block can be set for an
arbitrary size by changing the number of memory cell
transistors connected to the same source line. Besides
the case using the data line as a unit as typically
5 shown in Fig. 2 (the case where the common source line
is extended in the direction of the data line), a source
line division system includes also a case using the word
line as a unit (the case where the common source line is
extended in the direction of the word line). On the
10 other hand, simultaneous erase can be made for those
memory cells the control gates of which are connected in
common, in the erase operation of the negative voltage
system.

[2] Division into a plurality of memory blocks having
15 mutually different memory capacities

Fig. 3 is a block circuit diagram showing an
example of a flash memory including memory blocks which
are simultaneously erasable and have mutually different
memory capacities.

20 The flash memory FMRY1 shown in Fig. 3 has 8-
bits data input/output terminals D0 to D7, and is
equipped with memory cell arrays ARY0 to ARY7 for each
data input/output terminal. Each of the memory cell
arrays ARY0 to ARY7 is divided into a memory block LMB
25 having a relatively large memory capacity and a memory
block SMB having a relatively small memory capacity,
though this arrangement is not particularly limitative.
The diagram particularly illustrates details of the

1 memory cell array ARY0 as a typical example, but the
other memory cell arrays ARY1 to ARY7, too, have a
similar structure.

In each of the memory arrays ARY0 to ARY7,
5 memory cells MC each comprising an insulated gate field
effect transistor having the two-layered gate structure
explained with reference to Figs. 1A and 1B are arranged
in matrix. In Fig. 3, symbols WL0 to WLn represent word
lines which are in common to all the memory cell arrays
10 ARY0 to ARY7. The control gates of the memory cells
disposed on the same row are connected to the
corresponding word line. In each of the memory arrays
ARY0 to ARY7, the drain regions (first main electrodes)
of the memory cells MC disposed on the same column are
15 connected to the corresponding data line DL0 to DL7.
The source regions (second main electrodes) of the
memory cells MC constituting the memory block SMB are
connected in common to the source line SL1, and the
source regions of the memory cells MC constituting the
20 memory block LMB are connected in common to the source
line SL2.

A high voltage V_{pp} utilized for erase is
supplied from voltage output circuits VOUT1, VOUT2 to
the source lines SL1, SL2 described above. The
25 operation of the voltage output circuits VOUT1, VOUT2 is
selected in accordance with the value of bits B1, B2 of
an erase block designation register. For example, when
"1" is set for the bit B1 of the erase block designation

0043005 004098

1 register, only the small memory blocks SMB of the memory
cell arrays ARY0 to ARY7 can be simultaneously erased.
When "1" is set for the bit B2 of the erase block
designation register, only the large memory blocks LMB
5 of the memory cell arrays ARY0 to ARY7 can be
simultaneously erased. When "1" is set for both of the
bits B1 and B2, the flash memory can be simultaneously
erased as a whole.

Selection of the word lines WL0 to WLn

10 described above is effected when an X address decoder
XADEC decodes an X address signal AX fetched through an
X address buffer XABUFF and an X address latch XALAT. A
word driver WDRV drives the word line on the basis of a
select signal outputted from the X address decoder
15 XADEC. In the data read operation, the word driver WDRV
is operated using a voltage Vcc such as 5 V supplied
from a voltage select circuit VSEL and a ground
potential such as 0 V as the power source, drives the
to-be-selected word line to the select level by the
20 voltage Vcc and keeps the word line, which is not to be
selected, at a non-select level such as 0 V. In the
data write operation, the word driver WDRV is operated
using a voltage Vpp such as 12 V supplied from a voltage
selection circuit VSEL and the ground potential such as
25 0 V as the power source, and drives the to-be-selected
word line to a high voltage level for writing such as 12
V. In the data erase operation, the output of the word
driver WDRV is set to a low voltage level such as 0 V.

1 In each of the memory cell arrays ARY0 to ARY7, the data lines DL0 to DL7 are connected in common to the common data line CD through Y select switches YS0 to YS7.

Switch control of the Y select switches YS0 to YS7 is
5 effected when the Y address decoder YADEC decodes a Y address signal AY fetched through the Y address buffer YABUFF and the Y address latch YALAT. The output select signal of the Y address decoder YADEC is supplied in common to all the memory cell arrays ARY0 to ARY7.

10 Accordingly, when any one of the output select signals of the Y address decoder YADEC is set for the select level, the common data line CD is connected to one data line in each of the memory cell arrays ARY0 to ARY7.

The data read out from the memory cell MC to
15 the common data line CD is applied to a sense amplifier SA through the select switch RS, is amplified by this sense amplifier, and is then outputted outside from a data output buffer DOB through a data output latch DOL. The select switch RS is set for the select level in
20 synchronism with the read operation.

The write data supplied from outside is held by a data input latch DIL through a data input buffer DIB. When the data latched by the data input latch DIL is "0", the write circuit WR supplies a high voltage for
25 write to the common data line CD through the select switch WS. This high voltage for write is supplied through the data line selected by the Y address signal AY to the drain of the memory cell receiving the high

1 voltage at the control gate thereof by the X address
signal AX. In this way, this memory cell is written.
The select switch WS is set for the select level in
synchronism with the write operation.

5 Various timings for write/erase and select
control of the voltage are generated by a write/erase
control circuit WECONT.

There is a case where the data quantity to be
stored in the flash memory FMRY1 is different depending
10 on the usage of data and on the kinds of the data such
as a program, a data table, a control data, and so
forth. In consideration of such a case, a plurality of
memory blocks SMB, LMB having mutually different storage
capacities are provided as a simultaneously erasable
15 unit in the flash memory. According to such a
construction, any waste of the write operation
undesirably caused by simultaneous erase of all the
memory blocks for local or partial rewrite of the stored
data of the flash memory built-in in the microcomputer
20 after the microcomputer has been mounted onto a circuit
board, can be eliminated to improve the write
efficiency.

[3] Principle of data write in a flash memory by
command system by PROM writer

25 Fig. 4 is a functional block diagram when the
built-in flash memory of the microcomputer MCU1 (which
may be formed in a single semiconductor substrate)
having the flash memory FMR2, according to the first

1 embodiment of the present invention, is subjected to a
rewrite processing by a PROM writer.

Fig. 4 illustrates the central processing unit
(hereinafter also referred to merely as "CPU") 10, the
5 flash memory FMRY2 and the control circuit 20 as
exemplary circuit modules sharing the internal bus BUS.
This microcomputer MCU1 has a write operation mode by
use of the PROM writer 30. For example, when the
microcomputer MCU1 is connected to predetermined
10 terminals of the PROM writer 30 through a socket
adapter, not shown, the mode setting terminal, not
shown, of the microcomputer MCU1 is compulsively set for
a predetermined level, so that the operation mode of the
microcomputer MCU1 is set for the write mode by the PROM
15 writer 30 (ROM writer write mode operation). In such an
operation mode, the CPU 10 is cut off from the internal
bus BUS through a bus switch, not shown. In a state
where the write operation mode is set by the PROM writer
30, the control circuit 20 includes command latch 21
20 which is made writable from the PROM writer 30 and
serves to latch a command supplied from the PROM writer,
command analyzer 22 for analyzing (i.e., decoding)
the command latched in the command latch, and sequence
controller 23 for executing sequence control for
25 rewriting of the flash memory in accordance with the
analyzed content. The PROM writer 30 supplies
predetermined commands such as erase, erase verify,
program (write), program verify, etc., and suc-
cessively supplies necessary data and address data to

1 the control circuit 20. The command supplied from the
PROM writer 30 is interpreted by the command analyzer 22
and the sequence controller 23 applies to the flash memory
FMRY2 a control signal for a write operation utilizing the
5 necessary data and address data in accordance with the
interpretation by the analyzer 22.

As has been described above, the rewrite
(erase and write) sequence in accordance with commands
given from the PROM writer 30 can be accomplished by the
10 control circuit 20 included in the microcomputer MCU1 by
having the PROM writer 30 only to supply commands, before
supply of data and address information, to the
microcomputer MCU1 in the same way as the PROM writer 30
supplies the data thereto. Accordingly, by connecting
15 microcomputer MCU1 to the PROM writer 30 which is
generally utilized, through a socket adapter, data can
be written to the flash memory FMRY2 built-in in the
microcomputer. In this construction, the microcomputer
MCU1 in which the write mode by the PROM writer 30 is
20 set can be regarded as identical with a discrete flash
memory chip by the PROM writer 30.

Fig. 5 shows a functional block diagram of a
microcomputer MCU2 (which may be formed in a single
semiconductor substrate) having the flash memory FMRY2
25 built-in according to a second embodiment, in which a
rewrite processing is executed for the built-in flash
memory MRY2 by the PROM writer 30.

1 The microcomputer MCU2 shown in Fig. 5
eliminates the exclusive circuits for rewrite, such as
the command analyzer 22 and the sequence controller 23,
by allowing the built-in CPU 10 to execute the command
5 analysis and the sequence control without the control
circuit 20. In Fig. 5, since the CPU 10 is cut off from
the internal bus BUS during the write mode by the PROM
writer 30, there is no necessity for the built-in CPU 10
to execute a different processing during the rewrite
10 operation of the flash memory FMRY2 by the PROM writer
30, and therefore, it may be highly possible that the
CPU 10 is at halt or dormant, due to the disconnection
from the internal bus. The structure shown in Fig. 5
efficiently utilizes such built-in CPU 10.

15 Fig. 5 typically shows the CPU 10, the flash
memory FMRY2 and the command latches 21a to 21c as the
circuit modules sharing the internal bus BUS. This
microcomputer MCU2 has a write mode by the PROM writer
30. For example, when the microcomputer MCU2 is
20 connected to the predetermined terminals of the PROM
writer 30 through the socket adapter, not shown, the
mode setting terminal of the microcomputer MCU2, not
shown, is compulsively set for the predetermined level,
and the write mode by the PROM writer 30 is set. The
25 PROM writer 30 is disconnected from the internal bus BUS
so as not to directly supply the data and the address
information to the internal bus so that the supplied
information do not conflict with the internal bus access

1 by the CPU 10; however, the construction is not particu-
larly limited thereto. The command, data and the address
information are written in the command latch 21a, data
latch 21b and the address latch 21c, respectively. The
5 CPU 10 realizes, in the write operation mode by the PROM
writer 30, a function of the command analyzer 22 for
analyzing the command written from the PROM writer 30
and a function of the sequence controller 23 for
executing the sequence control for rewriting the flash
10 memory FMRY2 in accordance with the analyzed content, as
well as a control program for the functions. The PROM
writer 30 supplies to the latches 21a to 21c
predetermined commands such as erase, erase verify,
program (write), program verify, etc, and successively
15 supplies the necessary data information and address
information. The command supplied from the PROM writer
30 is interpreted by the CPU 10, and the CPU 10 sends a
control signal for the write operation to the flash
memory FMRY2 by utilizing the necessary data information
20 and address information written in the address latch 21b
and data latch 21c.

Figs. 6A to 6C show an example of a command
write timing by the PROM writer 30. In Fig. 6A, the
cycle labeled "command write cycle" is the write cycle
25 by the PROM writer 30 into the microcomputer MCU2.
First, the command is written in the command latch 21
and then, the data information and the address
information are written in the data latch 21c and the

28

T300x

ITEM	2ND EMBODIMENT (CPU CONTROL)	1ST EMBODIMENT (HARDWARE CONTROL)
SCALE OF CONTROL CIRCUIT	300 Trs.	3,200 Trs.
CHANGES OF COMMAND SPECIFICATION	SOFTWARE CHANGES	MASK CHANGES
CHANGES OF WRITE/ERASE CONDITIONS	SOFTWARE CHANGES	MASK CHANGES

SECRET

5

10

1 The CPU 10, the flash memory FMRY2, the random
access memory RAM and the 16-bit integrated timer/pulse
unit IPU are connected to the address bus ABUS, to a low
order data bus LDBUS (e.g. 8 bits) and to a high order
5 data bus HDBUS (e.g. 8 bits). The serial communication
interface SCI, the watch-dog timer WDTMR, the interrupt
controller IRCONT, the analog/digital converter ADC, the
wait state controller WSCONT and the ports PORT1 to
PORT12 are connected to the address bus ABUS and to the
10 high order data bus HDBUS.

 In Fig. 8, Vpp denotes a high voltage for
rewriting the flash memory FMRY2. EXTAL and XTAL denote
signals applied from an oscillator, which is externally
connected to the chip of the microcomputer MCU3 and is
15 not shown in the drawing, to the clock generator CPG
described above. ϕ denotes a sync clock signal
outputted outside from the clock generator CPG. RES*
(symbol * represents that the signal with this asterisk
is a low enable signal) is a reset signal, and STBY*
20 denotes a standby signal, and is supplied to the CPU 10
and to other circuit blocks. NMI denotes a non-maskable
interrupt signal, and applies a non-maskable interrupt
to the interrupt controller IRCONT. Other interrupt
signals not shown are given to the interrupt controller
25 IRCONT through the ports PORT8 and PORT 9. AS* denotes
an address strobe signal representing effectiveness of
the address signal outputted outside, RD* denotes a read
signal notifying to the outside that the operation cycle

1 is the read cycle, HWR* denotes an upper byte write
signal notifying to the outside that the operation cycle
is the write cycle of the high order 8 bits, and LWR*
denotes a lower byte write signal notifying to the
5 outside that the operation cycle is the write cycle of
the low order 8 bits. These signals are used as the
access control signals of the microcomputer MCU3 to the
outside.

MD0 to MD2 denote mode signals which are
10 supplied to the control circuit CONT so as to set the
operation mode of the microcomputer MCU3. The operation
modes set by such mode signals include, though not
particularly limitative, an operation mode relating to
the address space the CPU can manage, such as a maximum
15 mode and a minimum mode, and an operation mode which
makes it possible for the PROM writer 30 to write data
to the built-in flash memory FMRY2 (which will be merely
called the "PROM writer write mode"). In contrast with
this PROM writer write mode, the maximum mode and the
20 minimum mode described above can be understood to mean the
operation modes in which the CPU 10 makes the built-in
flash memory FMRY2 rewritable in the on-board state of
the microcomputer MCU3.

In the operation modes other than the
25 operation mode in which the data or information is
written in the flash memory FMRY2 by the PROM writer 30
in accordance with the command system, the ports PORT1
and PORT2 are allocated to the input/output operation of

1 the data BD0 to BD15 by the microcomputer MCU3 in order
to make an access to the outside, though this
arrangement is not particularly limitative. The ports
PORT3 to PORT5 are allocated to the output operation of
5 the address signals BA0 to BA19 at this time, though
this arrangement is not particularly limitative, either.

On the other hand, when the PROM writer write
mode is set in the microcomputer MCU, the ports PORT2 to
PORT5 and PORT8 are allocated to the connection with the
10 PROM writer 30 for the rewrite control of the flash
memory FMRY2 at this time, though this arrangement is
not particularly limitative. In other words, the port
PORT2 is allocated to command write and to input/output
of data ED0 to ED7 for data write and write verify, and
15 the ports PORT3 to PORT5 and PORT8 are allocated to
input of the address signal EA0 to EA16 and to input of
the access control signals CE* (chip enable signal),
OE* (output enable signal) and WE* (write enable
signal). The chip enable signal CE* is a chip select
20 signal from the PROM writer 30, the output enable signal
OE* is an instruction signal of the output operation for
the microcomputer MCU3, and the write enable signal WE*
is an instruction signal of the write operation for the
microcomputer MCU3. By the way, the input terminal of
25 the signal NMI is allocated to the input of one bit EA9
among the address signals EA0 to EA16. The external
terminals of the ports allocated in this way and other
necessary external terminals such as the terminal of the

1 ARY, the control gate of each memory cell is connected
to the corresponding word line, the drain region of the
memory cell is connected to the corresponding data line
and the source region of the memory cell is connected to
5 the common source line for each memory block in the same
way as in the structure which has been explained with
reference to Fig. 3. However, the mode of division of
the memory cell blocks may be different from that shown
in Fig. 3. As shown in Fig. 11, for example, it is
10 divided into seven large memory blocks (large blocks)
LMB0 to LMB6 having relatively large storage capacities
and eight small memory blocks (small blocks) SMB0 to
SMB7 having relatively small storage capacities. Each
large memory block is utilized for a program storage
15 region or a large capacity data storage region. Each
small memory block is utilized for a small capacity data
storage region.

In Fig. 10, AIL denotes a latch circuit for
the address signals PAB0 to PAB15. The address signals
20 PAB0 to PAB15 correspond to the output address signals
delivered to the address bus ABUS from the CPU 10, and
also correspond to the output address signals EA0 to
EA15 of the PROM writer 30 in the PROM writer write
mode, respectively. XADEC denotes the X address decoder
25 which decodes the X address signal fetched through the
address latch AIL. The word driver WDRV drives a word
line on the basis of the select signal outputted from
the X address decoder XADEC. In the data read

1 operation, the word driver drives the word line with a
voltage such as 5 V and in the data write operation, it
drives the word line with a high voltage such as 12 V.
In the data erase operation, all the outputs of the word
5 drivers are set for a low voltage level such as 0 V.

YADEC denotes a Y address decoder for decoding
the Y address signal fetched through the address latch
AIL. YSEL denotes a Y selector for selecting the data
line in accordance with the output select signal of the
10 Y address decoder YADEC. SA denotes a sense amplifier
for amplifying the read signal from the data line
selected by the Y selector YSEL in the data read
operation. DOL denotes a data output latch for holding
the output of the sense amplifier SA. DOB denotes a
15 data output buffer for outputting outside the data held
by the data output latch DOL.

In Fig. 10, PDB0 to PDB7 denote low order
eight-bit (one byte) data and PDB8 to PDB15 denote high
order eight-bit (one byte) data. According to this
20 embodiment, the output data is maximum two bytes. DIB
denotes a data input buffer for fetching the write data
supplied from outside. The data fetched from the data
input buffer DIB is held by the data input latch DIL.
When the data held by the data input latch DIL is "0",
25 the write circuit WR supplies a high voltage for write
to the data line selected by the Y selector YSEL. This
high voltage for write is supplied to the drain of the
memory cell, to the control gate of which a high voltage

1 is applied, in accordance with the X address signal, so
that this memory cell is written.

EC denotes an erase circuit for simultaneously
erasing the memory blocks by supplying an erase high
5 voltage to the source line of the designated memory
blocks. Designation of the erase blocks for the erase
circuit EC is made by an erase block designation register
MBREG. Writing of data in this register MBREG is carried
out by the CPU10.

10 FCONT denotes a controlling circuit for selec-
tively controlling the timing of the data readout opera-
tion in the flash memory FMRY2, various timings for write
and erase and selection of voltages. The controlling
circuit FCONT includes an erase block designation
15 register MBREG and a control register CREG. This con-
trolling circuit FCONT executes these processings by
referring to the content of the control register CREG.
In Fig. 10, the registers MBREG and CREG are shown out-
side the block of the circuit FCONT for convenience sake.

20 Figs. 12A to 12C show examples of the control
register CREG and the erase block designation register
MBREG described above. This erase block designation
register MBREG comprises two registers MBREG1 and MBREG2,
and each of the registers MBREG1, MBREG2 is an eight-bit
25 register. In the control register CREG, Vpp denotes a
high voltage application flag which is set for "1" for
application of the high voltage for rewrite. E bit is a
bit designating the erase operation, and EV bit

1 is a designation bit of a verify operation at the time of
an erase operation. P bit is a designation bit of the verify
operation at the time of the write operation (program
operation), and PV bit is a designation bit of the verify
5 operation at the time of a write operation. The erase block
designation registers MBREG1, MBREG2 are the registers
which designate which of memory blocks contained in the
large memory blocks divided into the seven blocks and in
the small memory blocks divided into the eight blocks
10 should be erased. The bits from the 0th bit to the
seventh bit are designation bits for each memory block.
For example, the bit "1" means the selection of the
corresponding memory block and the bit "0" means non-
selection of the corresponding memory block. When the
15 seventh bit of the erase block designation register
MBREG2 is "1", for example, erase of the small memory
block SMB7 is designated.

The registers CREG, MBREG1, MBREG2 are made
readable and writable by the CPU 10.

20 The controlling circuit FCONT refers to the
set contents of the registers CREG, MBREG1, MBREG2 and
executes erase and write. The CPU 10 can control the
erase and write operations by rewriting the contents of
the registers CREG, MBREG1, MBREG2. When the PROM
25 writer write mode described already is set, for example,
the CPU 10 sets the registers CREG, MBREG1, MBREG2 in
accordance with the contents of the commands written in
the command latch by the PROM writer 30.

1 In Fig. 10, FLM, MS-FLN, MS-MISN, M2RDN,
M2WRN, MRDN, NWRN, IOWORDN, RST, VPPH, A9H, SECSN, SECN,
DSCN and XMON are supplied as the control signals to the
controlling circuit FCONT.

5 The control signal FLM is the signal which
designates the operation mode of the flash memory FMRY2,
and is set for the logic value "1" when the
microcomputer MCU3 is connected to the PROM writer 30
and is made rewritable, and for the logic value "0" at
10 other times. This signal FLM is generated on the basis
of the mode signals MD0 to MD2 described above, for
example. The control signal MS-FLN is the select signal
for selection of the flash memory FMRY2. The control
signal MS-MISN is the select signal of the registers
15 CREG, MBREG1, MBREG2. Which of these registers CREG,
MBREG1, MBREG2 should be selected is decided by the low
order two bits (PAB0 and PAB1) of the address signal
outputted from the CPU 10, M2RDN denotes the memory read
strobe signal, M2WRN denotes the memory write strobe
20 signal, MRDN denotes the read signal for reading from the
control register CREG, MWRN denotes the write signal for
writing in the control register CREG. The memory write
strobe signal M2WRN is regarded as the strobe signal for
writing the data, which is to be written in the memory
25 cells, in the data input latch DIL. The practical write
operation into the memory cells is started when the P
bit of the control register CREG is set. The control
signal IOWORDN denotes a switch signal of the eight-bit

1 read access and the sixteen-bit read access for the
flash memory FMRY2. The control signal RST denotes a
reset signal of the flash memory FMRY2. When this
signal RST resets the flash memory FMRY2 or when the Vpp
5 flag of the control register CREG is set for "0", each
mode setting bit of EV, PV, E and P in the register CREG
is cleared. VPPH denotes a detection signal indicating
that Vpp = 12 V is detected. By the way, other signals
A9H, SECN, DSCN and XMON are enable signals and test
10 enable signals of the security bits, and since they are
not directly relevant to the present invention, their
detailed explanation will be omitted.

[6] Hardware adapted to command system

Fig. 13 shows details of hardware for
15 facilitating the PROM writer rewrite mode by the command
system in the microcomputer shown in Fig. 8. The
hardware are implemented within a single semiconductor
substrate 1.

The command and the address that are supplied
20 from the PROM writer 30 are asynchronously inputted with
respect to the CPU 10. Therefore, the command latch CL
for receiving the command and the address latch AL for
receiving the address are provided. The port PORT to be
connected to the PROM writer 30 is primarily determined
25 through the socket adapter, not shown in the drawing.
When the port PORT has a register, the register can be
used as the address latch AL and the command latch CL,
and they may not be provided separately. A command flag

1 CF is allocated to a predetermined bit of the command
latch CL so that the CPU 10 can recognize write of the
command into the command latch CL. When the command
flag CF is set up, the CPU 10 can know that the command
5 is inputted to the command latch CL, and then reads the
command. In the write operation by the PROM 30, the
write operation of the command is first made and then,
the address and the data are written in the address
latch AL and the data latch from the PROM writer 30,
10 whenever necessary. At this time, since the time from
the command input to the data input is as short as
minimum 20 ns, there may be a case where the data is
inputted to the command latch CL before the CPU 10 reads
the command. Therefore, to avoid collision between the
15 command and the data, the data latch DL for receiving
the data is provided besides the command latch CL.
Further, a data flag DF representing that the data is
inputted to the data latch DL is allocated to a
predetermined bit of the command latch. In the case of
20 CF = 1 (representing that the command has already been
inputted) or DF = 1 (representing that the command has
already been inputted and furthermore, the data has also
been inputted already), the CPU 10 reads the command,
and reads the data after recognition of the command in
25 the case of DF = 1.

Here, the two latches, that is, the command
latch CL and the data latch DL, share the data
input/output port PORT. Therefore, the command and the

1 data inputted from the PROGM writer 30 must be
discriminated. For this reason, the input data from the
PROM writer 30 is latched in the command latch CL when
CF = 0 and DF = 0, and is latched in the data latch DL
5 when CF = 1 and DF = 0. In other words, as shown
conceptually in Fig. 13, there is provided an AND gate
AND which receives the signal corresponding to the logic
values of the write signal WE*, the command flag CF and
the data flag DF from the PROM writer 30 and generates
10 latch control signals.

Further, as shown in Fig. 14, too, this
embodiment employs the logic such that the kind of the
command latched by the command latch CL is decoded by
the decoder DEC, the command flag CF is set when the
15 command is a predetermined command, and the data flag DF
is set and moreover, the command flag CF is cleared when
the data is latched in the data latch DL. In this way,
the separate use of the command latch CL and the data
latch DL can be accomplished. According to this
20 embodiment, the command latch CL is the eight-bit
register, the low order two bits are the data flag DF
and the command flag CF and the high order four bits are
command latch bits. By the way, AIB in Fig. 13 denotes
an address input buffer and MPX denotes an address
25 multiplexer.

As described above, the command latched in the
command latch CL is decoded by the command decoder DEC
and the command flag CF is set. If this processing is

1 handed over to the CPU 10, the CPU 10 must always
monitor the content of the command latch CL by activat-
ing the bus cycle, and in this case, a waste of opera-
tion takes place. Further, if the CPU 10 must analyze
5 all the commands of the command latch CL in accordance
with the set condition of the command flag CF which is
controlled by the command decoder DEC, the timing of the
operation designated by the command may be too late. An
example is the read command which reads out the data
10 from the flash memory FMRY2. To cope with this problem,
there is provided, inside the internal buses ABUS, DBUS,
bus switches BSW1 and BSW2 capable of selectively
establishing a state where the command latch CL, the
data latch DL and the address latch AL are connected to
15 the flash memory FMRY2 and a state where the command
latch CL, the data latch DL and the address latch AL are
not connected to the flash memory FMRY2 as shown in
Figs. 13 and 14, and these bus switches BSW1 and BSW2
are controlled by the signal obtained by the decoding
20 result of the read type commands by the decoder DEC.
When the bus switches BSW1 and BSW2 are opened, a direct
read access can be made to the flash memory from outside
the microcomputer MCU3 or in other words, from the PROM
writer 30.

25 [7] Command specification data write and others in a
flash memory by PROM writer

Table 3 shows examples of the command specifi-
cation which may be supplied from the PROM writer 30.

Table 3

COMMAND	CYCLE NUMBER	1ST CYCLE			2ND CYCLE		
		MODE	ADDRESS	DATA	MODE	ADDRESS	DATA
READ	2	WRITE	X	00H	READ	RA	DOUT
READ ID	2	WRITE	X	90H	READ	IA	ID
ERASE	2	WRITE	X	20H	WRITE	X	20H
E VERIFY	2	WRITE	X	A0H	READ	X	EVD
A ERASE	2	WRITE	EA	30H	WRITE	X	30H
PROGRAM	2	WRITE	X	40H	WRITE	PA	PD
P VERIFY	2	WRITE	X	COH	READ	X	PVD
RESET	2	WRITE	X	FFH	WRITE	X	FFH

- 1 The commands shown in the table are eight kinds, though this number is not particularly limited. The content of the cycle to be activated by the PROM writer 30 in response to each command is also shown. The code of the
- 5 command corresponds to the data of the first cycle shown in the table. This code is represented by the hexadecimal number and symbol H put at the end of the code means the hexadecimal number. The read command (Read) is the command for reading out the data from the flash
- 10 memory FMRY2. Symbol RA in the second cycle of this command means the read address. The read ID command (Read ID) is the command for reading out a product identification code (ID) from a product identification code address (IA). The erase command (Erase) is the
- 15 command for erasing the data of the flash memory. To avoid over-erase (the phenomenon in which Vth of the

00132005"004000

1 memory becomes negative due to excessive erase and
normal read-out cannot be made) during erasing, pre-
write is executed for making a write level uniform before
beginning the erasing operation, or an erase procedure
5 which effects erasure little by little while effecting
verify is employed. The erase verify command (E Verify)
is the command for confirming the erase condition. EA
represents the memory address for erase verify. EVD
represents the erase verify output data. The automatic
10 erase mode (A Erase) is the command for automatically
executing erase and erase verify, and after the
automatic erase is started, the end of this automatic
erasing operation is confirmed by a status polling. A
status polling flag SPF is allocated to the high order
15 side bit of the data latch DL shown in Fig. 13. The
write command (Program) is the command for designating
write, PA represents the write address and PD represents
the write data. A program verify command (P Verify) is
the command for confirming whether or not the data
20 written immediately before is written correctly, and PVD
represents a program verify output data. A reset
command (Reset) is the command for resetting the command
when this command is mistaken.

The command specification described above has
25 compatibility with the command specification of discrete
flash memory LSIs (1M-bit flash memory) of an HN28F101
series described on page 872 of "Hitachi IC Memory Data

45

1 Book 1" published in September, 1991, though the
specification is not particularly limited.

[8] Data write in a flash memory in on-board state

The designation of the data write in the on-
5 board state and its sequence are all controlled by the
CPU 10 and its operation program, and processing such as
data write is controlled by setting/clearing each bit of
the control register CREG by the software. When the
rewrite program is placed on the flash memory FMRY2, for
10 example, the rewrite program is in advance transferred
to the RAM at the time of the data write operation or at
the time of resetting of the system, and the CPU 10
executes this program on the RAM so as to execute data
rewrite. An example of the sequence of this rewrite
15 processing will be hereinafter described in this item.

The data write in the flash memory is
basically effected to the memory cells in an erase
state. When rewrite of the flash memory included in the
microcomputer is carried out in a state where the
20 microcomputer is mounted onto the system, the rewrite
control program to be executed by the CPU 10 includes
the erase program and the write program. This rewrite
control program can be constituted in such a manner that
the erase processing routine is first executed and then
25 the automatic write processing routine is successively
executed in accordance with the data write instruction.
Alternatively, the erase operation and the write
operation may be separately designated.

1 Figs. 15A and 15B show a detailed example of
the write control procedure. The control main body of
the procedure shown in the drawings is the CPU 10.

In the first step of writing data in the byte
5 unit, the CPU 10 sets 1 to its built-in counter n (Step
S1). Next, the CPU 10 sets the data to be written in
the flash memory FMRY2, in the data input latch DIL
shown in Fig. 13 and sets the write address in the
address latch AIL (Step S2). Then, the CPU 10 issues
10 the write cycle for the control register CREG and sets
the program bit P (Step S3). The controlling circuit
FCONT applies a high voltage to the control gate and the
drain of the memory cell designated by the address on
the basis of the data and the address that are set in
15 the Step S2, and executes write. The CPU 10 is in the
waiting state for the time (x) μ sec as the write
processing time on the flash memory side (Step S4), and
then clears the program bit P (Step S5). Here, the time
(x) μ sec is determined in accordance with the character-
20 istics of the memory cell and is 10 μ sec, for example.

Thereafter, the CPU 10 issues the write cycle
for the control register CREG to confirm the write state
and sets the program verify bit PV (Step S6). The
controlling circuit FCONT utilizes the address set by
25 the Step S2, applies the verify voltage to the word line
to be selected by the address and reads out the data of
the memory cell which is written as described above.
CPU 10 waits for (y) μ sec for this data read out (Step

1 S7). Here, to insure a sufficient write level, the
verify voltage is at a voltage level of 7 V higher than
the power source voltage of 5 V, for example. The time
(y) μ sec is determined by the rise characteristics of
5 such a verify power source, and is below 2 μ sec, for
example. The CPU 10 confirms coincidence between the
data thus read out and the data used for write (Step
S8). When the CPU 10 confirms this coincidence by
verify, it clears the program verify bit PV (Step S9)
10 and in this way, the write operation of this one-byte
data is completed.

On the other hand, when the CPU 10 confirms inequality by verify in the Step S8, it clears the program verify bit PV in the Step S10, and then judges whether or not the value of the counter n reaches the upper limit number N of the write re-try (Step S11). When this upper limit number N of the write re-try is reached, the processing is completed as write fault. When the upper limit number N is not reached, the CPU 10 increments by one the value of the counter n (Step S12), and repeats the processing from the Step S3 described above.

Figs. 16A and 16B show a detailed example of the erase control procedure. The control main body of the procedure shown in the drawings is the CPU 10.

To effect erase, the CPU 10 sets 1 in its built-in counter n (Step S21). Next, the CPU 10 executes pre-write in the memory cells in the region to

1 be erased (Step S22). In other words, the CPU 10 writes
the data "0" in the memory cell of the address where
erase is to be effected. The control procedure of this
pre-write can use the write control procedure explained
5 with reference to Figs. 15A and 15B. This pre-write
processing is made so as to make uniform the charge
quantity inside the floating gate before erase
throughout all the bits to thereby make uniform the
erase state of each memory cell to be erased.

10 Next, the CPU 10 issues the write cycle for
the erase block designation registers MBREG and
designates the memory blocks as the simultaneous erase
object (Step S23). In other words, the CPU 10
designates the number of memory blocks to be erased to
15 the erase block designation registers MBREG1 and MBREG2.
After the memory blocks to be erased are designated, the
CPU 10 issues the write cycle for the control register
CREG and sets the erase bit E (Step S24). The
controlling circuit FCONT applies the high voltage to
20 the source line of the memory blocks designated in the
Step S23 and simultaneously erases the memory blocks.
The CPU 10 waits for the time of (x) msec (Step S25).
Here, the time (x) msec is determined to match with the
characteristics of the memory cell transistors, and is
25 10 msec, for example. This time (x) msec is shorter
than the time in which the erase operation can once be
completed. Next, the erase bit E is cleared (Step S26).

Next, to confirm the erase condition, the CPU

1 10 sets the leading addresses of the memory blocks to be
simultaneously erased for the address to be verified
(Step S27), and then executes dummy write to the verify
address (Step S28). In other words, the CPU 10 issues
5 the memory write cycle to the address to be verified.
In consequence, the memory address to be verified is
latched in the address latch AIL. Thereafter, the CPU
10 issues the write cycle for the control register CREG
and sets the erase verify bit EV (Step S29). Utilizing
10 the address set in the Step S28, the controlling circuit
FCONT applies the erase verify voltage to the word line
to be selected and reads out the data of the memory cell
which is to have been erased as described above. To
read the data, the CPU 10 waits for time (y) μ sec (Step
15 S30). To insure a sufficient erase level, the erase
verify voltage is set for a voltage level of 3.5 V, for
example, which is lower than the power source voltage
Vcc such as 5 V, for example. The time (y) μ sec is
determined by the rise characteristics of the verify
20 power source and is the time of shorter than 2 μ sec, for
example. The CPU 10 verifies whether or not the data
read by it coincides with the data under the erase
completion state (all "1" bit state) (Step S31). After
confirming the coincidence by this verify, the CPU 10
25 clears the erase verify bit EV (Step S32). Next,
whether or not the verify address of this time coincides
with the final address of the erased memory block is
judged (Step S33), and if it is, the series of the erase

1 operation is completed. When it is not judged as
reaching the final address, the verify address is
incremented by one (Step S34), and the processing from
the Step S28 is again repeated.

5 On the other hand, when the CPU 10 confirms
inequality by the verify operation in the Step S31, it
clears the erase verify bit EV in the Step S35 and then
judges whether or not the value of the counter n has reached
progressively the upper limit number N of erase (Step
10 S36). If this upper limit number N is reached, the
processing is completed as an erase fault. If the upper
limit number N is not reached, the CPU 10 increments the
value of the counter by one (Step S37) and repeats the
processing from the Step S24. In order to prevent over-
15 erase in which the threshold voltage of the memory cell
becomes negative, erase is gradually repeated in
practice every time within a short time such as 10 msec
by effecting verify each time.

[9] Data write operation by command system

20 When the data write mode by the PROM writer is
set in the microcomputer MCU3 through the mode signals
MDO to MD2, the data is written in the flash memory
FMRY2 by the PROM writer 30 by the system referred to as
the "command system". Here, the term "command system"
25 means a system in which a command such as for data writing
in the flash memory is given by such command from an
external device such as the PROM writer 30. The CPU 10
controls the processing based on the command. The

51

1 control program for this purpose is stored in the flash
memory FMRY2, and this program is transferred to the RAM
in response to setting of the data write mode by the
PROM writer 30. The CPU 10 executes the control program
5 thus transferred to the RAM. This control program may
be partly in common to the program for controlling the
data write in the built-in flash memory in the on-board
state described already, or may be entirely different.
The command specification has already been explained
10 with reference to Table 3. Hereinafter, the operation
will be explained for each command.

(1) Write command (PROGRAM)

The PROM writer 30 writes, asynchronously with
respect to the CPU 10, the command, the data and the
15 address in the command latch CL, the data latch DL and
the address latch AL shown in Fig. 13, respectively, in
accordance with the command specification shown in Table
3. When the command flag CF is CF = 1 (the command has
already been inputted) or when the data flag DF is DF =
20 1 (the command has been inputted and further, the data
has been inputted), the CPU 10 reads the command, and
when the data flag is DF = 1 after recognition of the
command, it reads the data and the address. The command
supplied from the PROM writer 30 is latched in the
25 command latch CL in accordance with the command flag CF
= 0 and the data flag DF = 0. The data to be written in
the memory cell is latched in the data latch DL in
accordance with the command flag CF = 1 and the data

1 flag DF = 0. After recognizing that the command, which
is read, is the "write command", the CPU 10 reads the
address and the data from the address latch AL and the
data latch DL, respectively, and transfers them to the
5 address input latch AIL and the data input latch DIL
inside the flash memory FMRY2, respectively, according
to their control programs. The CPU 10 practically
executes write in the memory cell of the flash memory
FMRY2 by setting the write bit (P bit) of the control
10 register CREG. The procedure for the practical write
processing into the memory cell is substantially the
same as the procedure which has been explained with
reference to Figs. 15A and 15B. After the write
operation is made, the P bit is cleared, and CF and DF
15 are returned to 0. Fig. 17 altogether shows states of
the flags CF and DF in the write operation as well as
the operation of the CPU 10.

(2) Write verify command (P VERIFY)

After the write operation is completed, the
20 write verify mode is essentially executed. This write
verify is the operation which confirms whether or not
the data written immediately before is certainly
written. In the case of this command, too, the
operation up to the analysis of the command is executed
25 in the same way as in the write command described above.
After confirming that the command is the write verify
command, the CPU 10 effects the control in accordance
with the following procedure. First, the CPU 10 sets

00132005 "001000" 000T00

1 the PV bit (program verify bit) of the control register
CREG to "1". At this time, the address used for the
write operation immediately before is latched in the
address latch AIL inside the flash memory FMRY2.
5 Accordingly, the verify voltage (such as 7 V) is applied
to the word line selected by this address. Next, the
CPU 10 reads the flash memory FMRY2. In this case, too,
the latched address is used as the address. After all,
the read operation is executed in the state where the
10 verify voltage is applied as the gate voltage to the
memory cell in which write is previously made. The CPU
10 writes this read data in the data latch DL of the
port PORT, clears the PV bit and completes the
operation. The PROM writer 30 executes verify by reading
15 the value of the data latch DL. Fig. 18 altogether
shows states of the flags at the time of verify and the
operation of the CPU 10 at this time.

(3) Erase command (ERASE)

In the microcomputer MCU3 according to this
20 embodiment, the erase operation of the built-in flash
memory FMRY2 in the microcomputer MCU3 does not support
block erase but only simultaneous erase of a memory cell
array (one of ARY0, ARY1, shown in Fig. 3, for example)
so that the built-in flash memory is compatible with a 1
25 M flash memory (HN28F101) in the form of a discrete
flash memory LSI described already. As is obvious from
the command specification shown in Table 3, the erase
operation is started when the erase command is written

54

00133006"004000

1 twice. In the case of erase, too, the operation up to
the command analysis is the same as that of the write
operation. This erase is started by setting all the
bits of the erase block designation registers MBREG1 and
5 MBREG2 for a select state and then setting the E bit
(erase bit) of the control register CREG for "1". When
the E bit is set, the high voltage is applied to the
memory cell array and erase is carried out. After the E
bit is set for "1" for a predetermined time, it is
10 cleared and erase is completed. The control procedure
of erase of the memory cell is substantially the same as
the control content explained with reference to Figs.
16A and 16B.

(4) Erase verify command (E VERIFY)

15 The verify operation which is executed after
erase is similar to the write verify operation. After
the command analysis, the CPU 10 reads the address to be
verified from the address latch AL of the port and
writes it in the flash memory FMRY2. Next, the CPU 10
20 sets the EV bit of the control register CREG, so that
the verify voltage (such as 3.5 V) is applied to the
word line selected by the address latched previously.
The CPU 10 reads the flash memory FMRY2 in this state,
and writes the read data to the data latch DL of the
25 port. Thereafter, the EV bit is cleared and the verify
operation is completed.

(5) Automatic erase command (A ERASE)

After recognizing the automatic erase command,

55

1 the CPU 10 executes by itself all the erase flows shown
in Figs. 16A and 16B. In this automatic erase, the
flash memory FMRY2 outputs the status polling signal
simultaneously with the start of erase, and inverses the
5 signal upon completion of erase. Since the output of
the status polling is ED7 (Fig. 8), the seventh bit of
the data latch DL (Fig. 13) is used as the bit for
storing the status polling signal. The CPU 10 clears the
seventh bit (the most significant bit) of the data latch
10 DL simultaneously with the start of erase, and sets upon
completion of erase.

(6) Read command (READ)

When the read command (read type command) is
issued, the flash memory FMRY2 must be brought into a
15 state where it can be freely read from the PROM writer
30. When the CPU 10 interprets the command, the time
from the input of the command till the point at which
the command becomes readable becomes extended and cannot
match with the specification of the 1M flash memory.
20 Therefore, the CPU 10 is cut off by the bus switches
BSW1 and BSW2 (Fig. 13) in the read mode, and a direct
access is permitted from outside to the built-in flash
memory FMRY2. The CPU 10 is allowed to input a BREQ
(bus request) signal for requesting bus privilege to
25 open from outside, but the bus switches BSW1 and BSW2
physically cut off the bus because a long time is
necessary before the CPU 10 opens the bus. Since a long

56

1 time is necessary if all the commands are passed through
the CPU 10, the CPU 10 is instantaneously cut off as
soon as the decoder DEC (Fig. 13) recognizes the
commands as the read commands. In this case, in order
5 to prevent the CPU 10 from recognizing the input of the
command, the command flag CF is kept as $CF = 0$ in the
case of the read command, and the command flag $CF = 0$ is
changed to the command flag $CF = 1$ only in the case of
the other commands.

10 (7) Reset command (RESET)

The reset command is prepared to cope with the
case where setup of the command is mistaken. As is
obvious from the command specification shown in Table 3,
reset is completed when this reset command is written
15 twice. If any command is inputted at first and then the
command is again inputted in the microcomputer MCU3
according to this embodiment, the command is inputted to
the data latch DL. Therefore, there is a possibility
that the reset command first written is recognized as
20 the data FFH. However, since the flash memory regards
the erase state, where the electrons are extracted from
the floating gate, as "1", FFH becomes equal to the
state where nothing is written, even though the write
command has been inputted beforehand, and there is no
25 problem at all. When the reset command written at the
second time is decoded by the command decoder DEC, the
mode is brought into the read state as such in the same
way as in the read mode, and the operation is completed.

1 Figs. 19A and 19B altogether show states of the flags in
such a reset state and the operation of the CPU 10.

[10] Operation of PROM writer 30 for data write by
command system

5 Figs. 20A and 20B show the operation flow
charts of the PROM writer 30 during the data write
operation. First, the high voltage necessary for write,
such as 12 V, is applied to the terminal Vpp (Fig. 8)
(Step S40) so as to initialize the built-in address
10 counter to 0 (Step S41) and to set the counter n for 0
(Step S42). Next, the counter n is incremented by one
(Step S43), and then the write cycle of the program is
activated so as to write the write command (40H) into
the command latch CL (Step S44). The write data (PD)
15 and the write address are written into the data latch DL
and the address latch AL, respectively (Step S45).
Thereafter, the PROM writer waits for a time of 25 μ sec,
for example (Step S46). In the interim, the CPU 10 of
the microcomputer interprets the command and writes the
20 data in the flash memory FMRY2. The write cycle of the
write verify command is activated this time (Step S47),
and the PROM writer 30 waits for a time of 6 μ sec, for
example (Step S48). In the interim, the CPU 10 of the
microcomputer MCU 3 interprets this command and reads
25 out the data of the write address in the data latch DL.
The PROM writer 30 takes in this read data and judges
whether or not write can be effected normally (Step
S49). When the result of judgement proves normal,

1 whether or not it is the last write address is judged
(Step S50). If it is not the last address, the write
address is incremented (Step S51) and the flow then
returns to the Step S42. After write is made to the
5 last address, the high voltage Vcc such as 5 V is
applied to the terminal Vpp (Step S52) and write is
completed. When any write abnormality is judged in the
Step S49, the flow returns again to the Step S43 and
write is repeated until the value of the counter n
10 reaches maximum 20, for example. If this write ab-
normality cannot be solved even after this write opera-
tion is repeated twenty times, the processing is com-
pleted by regarding this address as the defective bit.

Figs. 21A and 21B show the operation flow
15 charts of the PROM writer 30 during the erase operation.
First, the data of the logic value 0 is written in all
the erase object bits of the flash memory. The write pro-
cessing is made in accordance with the flowcharts shown in
Figs. 20A and 20B. Next, the leading address of the
20 erase region is set in the address counter (Step S61)
and the counter n is set for 0 (Step S62). Next, the
counter n is incremented by one (Step S63) and then the
erase command (20H) is written in the command latch CL
by activating the write cycle of the erase command (Step
25 S64). Thereafter, the PROM writer 30 waits for a time
of 10 msec, for example (Step S65). In the interim, the
CPU 10 of the microcomputer MCU3 interprets the command
and erases the flash memory FMRY2. The write cycle of

1 the erase verify command is activated this time (Step
S66) and the PROM writer 30 waits for a time of 6 μ sec,
for example (Step S67). In the interim, the CPU 10 of
the microcomputer MCU3 interprets the command, reads out
5 the data from the erase verify address (EA) and transfers
the data to the data latch DL. The PROM writer 30 inputs
this read data and judges whether or not erase can be
effected normally (Step S68). When the result of judgement
proves normal, a judgement is effected as to whether or not the
10 present erase verify address is the last address (Step S69). If
it is not the last address, the erase verify address is incre-
mented (Step S70) and then the flow returns to the Step S66.
Erase verify is then carried out until the last address
and the processing is completed. If erase abnormality
15 is judged in the Step S68, the flow returns again to the
Step S63 and erase is repeated until the value of the
counter n reaches maximum 3,000, for example. When this
erase abnormality cannot yet be solved even after
repetition of 3,000 times, the processing is completed
20 by regarding the address as the defective bit.

[11] Operation of CPU for data write by command system

Fig. 22 shows a main flowchart of the
processing by the CPU 10 for various commands described
above. The CPU 10 performs polling of the command flag
25 CF and the data flag DF, and upon detecting their set
state, the CPU 10 reads the high order four bits of the
command latch CL (Fig. 14) and analyzes the command.

1 The processing routine branches to Erase Verify when the
command is A0H, to Write Verify (Program Verify) when it
is C0H, to write (Program) when it is 40H, to erase when
it is 20H, and to automatic erase (Auto Erase) when it
5 is 30H. By the way, the explanation of other commands
explained with reference to Table 3 will be omitted.

In the processing routine of Erase, the
sequence necessary for erasing the flash memory is
controlled as shown in Fig. 23A, the command flag CF is
10 cleared and then the processing is completed.

In the processing routine of Erase Verify
shown in Fig. 23B, the erase verify address is fetched
from the address latch AL, the erase verify mode is set
in the control register CREG, and the data from this
15 address is read and transferred to the data latch DL.

In the processing routine of Automatic Erase,
control of pre-write execution is made for all the
addresses of the built-in flash memory FMRY2 (to be
subjected to erase) as shown in Fig. 24, erase control
20 is then made, and erase verify is executed. Control of
erase and erase verify is made till completion of erase
of all the addresses (to be subjected to erase). When
erase abnormality repeatedly occurs and exceeds the
upper limit of the erase time in the judgement of the
25 erase condition, the processing is completed with the
existence of the defective bit.

In the processing routine of Program, the set
state of the data flag DF is judged as shown in Fig.

1 25A, the write address is fetched from the address latch
AL, the write data is fetched from the data latch DL,
write is made in the flash memory FMRY2, and thereafter
the processing is completed by clearing the data
5 flag DF.

In the processing routine of Program Verify,
the program verify mode is set in the control register
CREG as shown in Fig. 25B and the data is read out from
the write address immediately before, and is transferred
10 to the data latch DL. Further, the command flag CF is
cleared and the processing is completed.

[12] Compatibility between a flash memory built-in in a
data processing apparatus and a discrete flash
memory LSI in terms of write specification, as
15 seen from PROM writer

The inventors of the present invention have
confirmed compatibility between the specification for
writing data in a built-in flash memory FMRY2 by the
command system utilizing the PROM writer 30 and the
20 specification for writing the data in a discrete flash
memory LSI (HN28F101) using the PROM writer 30.
According to the inventors' investigation, various
timings must match with the 1M flash memory in order to
establish compatibility of data write by the PROM writer
25 30 with the 1M flash memory discrete LSI (HN28F101)
described above. Therefore, investigation has been
carried out by practically preparing the control program
to examine whether matching of the timings can be

1 obtained. The result of the investigation is shown in Table 4. It has been confirmed from the result of the investigation that compatibility can be obtained at an operation frequency of 16 MHz, for example.

Table 4

Response time from write of command in command latch to start of actual operation responsive to the written command

ITEM	ERASE VERIFY	WRITE VERIFY	ERASE	WRITE
RESPONSE TIME BY SOFTWARE CONTROL (OPERATION FREQUENCY: 16 MHz) ACCORDING TO EMBODIMENT	4.7 μ s	4.8 μ s	5.9 μ s	5.7 μ s
RESPONSE TIME REQUIRED FOR 1M FLASH MEMORY COMPATIBLE SPECIFICATION	5 μ s OR LESS	5 μ s OR LESS	1 ms OR LESS	10 μ s OR LESS
JUDGEMENT	○	○	○	○

5 The embodiments described above provide the following functional effects.

(1) The rewrite sequence in accordance with the commands asynchronously given from the PROM writer 30 is accomplished by the built-in circuit of the
10 microcomputer. Therefore, it is only necessary for the PROM writer 30 to write the commands in the command

1 latch in the same way as it gives the data, before the
data and the address data are given. Accordingly, data
writing can be effected in the flash memory built-in in the
microcomputer by connecting the PROM writer 30, which is
5 used widely, through the socket adapter.

(2) The built-in CPU 10 is caused to control the
rewrite sequence given by the commands. Therefore, the
exclusive circuit for only this control can be
eliminated or the number of such circuits can be
10 reduced, and the chip area of the microcomputer can be
reduced. Furthermore, the control sequence for rewrite
can be changed by the software which the CPU 10 should
execute. Accordingly, setting of the conditions such as
the write time can be easily effected so as to match with
15 the characteristics of the memory devices constituting the
flash memory.

(3) The PROM writer 30 versatily utilized is so
constituted as to apply at least the high voltage for
rewrite for the nonvolatile memory device and to supply
20 the address and the data for rewrite in accordance with
the write signal, etc, to the object semiconductor
device (LSI) inclusive of the flash memory. Such a PROM
writer 30 supplies, asynchronously with the CPU 10
built-in in the microcomputer, the commands, the data
25 and the addresses. At this time, there are provided the
command flag CF representing that the command is written
in the command latch CL, and the data latch DL which is
made writable from outside in addition to the command

1 latch CL when this command flag CF represents the
command latch state. In this way, collision can be
prevented between the commands and the data that are
written from the PROM writer 30 in mutually different
5 cycles, on the latch means.

(4) The CPU 10 reads the command of the command
latch on the basis of the command latch state of the
command flag CF. At this time, the set processing of
the command flag can be speeded up because there is
10 provided the command decoder for decoding the latch
content of the command latch CL and setting the command
flag CF for the command latch state. If the control for
the command flag is also assigned to the CPU 10, the CPU
10 must activate the bus cycle and must always monitor
15 the content of the command latch CL, so that a wasteful
operation undesirably occurs and the flag processing
becomes delayed, as well.

(5) The present invention provides the bus
switches BSW1 and BSW2 which cut off the CPU 10 from the
20 flash memory in accordance with the decoding result of
the read commands by the command decoder DEC. If the
CPU 10 were to analyze all the commands latched in the
command latch, the timing of the operation designated by
the command would be retarded. However, the present
25 invention can easily cope with the read commands due to
the bus switches. This makes it possible to accomplish
compatibility, with respect to the write processing,
between the discrete flash memory LSI and the flash

1 memory built-in in the microcomputer, as seen from the
PROM writer 30.

(6) The program for controlling the rewrite
procedure of the flash memory, which is to be executed
5 by the CPU 10, is stored in the flash memory and is
transferred to the RAM in response to setting of the
rewrite mode by the PROM writer 30. The CPU 10 executes
this program transferred to the RAM and, in this way,
correction of the rewrite program can be made.

10 (7) In view of the fact that the quantity of data
to be stored in the flash memory becomes different
depending on the usage of the data and on the kind of
data employed such as the program, the data table, the
control data and so forth, a plurality of memory blocks
15 having mutually different memory capacities are provided
as a simultaneously erasable unit in the flash memory
and in this way, a waste in the write operation caused
by simultaneous erase of the memory blocks for local or
partial rewrite of the data held in the built-in flash
20 memory after mounting onto the system can be eliminated
to improve the rewrite efficiency.

Although the invention has thus been described
specifically on the basis of the embodiments thereof,
the invention is not particularly limited thereto but
25 can of course be effected via other embodiments and/or
various modifications thereof including with respect to
thus far disclosed embodiments and schemes without depart-
ing from the scope thereof.

For example, the peripheral circuits built-in
the microcomputer are not limited to those of the

1 embodiments described above, but can be suitably
changed. The memory cell transistors of the flash
memory are not limited to the stacked gate structure MOS
transistors of the embodiments described above, and
5 FLOTOX type memory cell transistors utilizing the tunnel
phenomenon for the write operation may be employed.

Besides the memory blocks sharing the source
line in common, those memory blocks which can share the
word line in erase can be used as the unit of
10 simultaneous erase. Which of them is to be used is
determined by considering the polarity of the erase
voltage or by considering which of the number of memory
cells to be connected to a single word line and the
number of memory cells to be connected to a single data
15 line is smaller when the memory capacity of the
simultaneous erase unit is minimized.

The size of the memory blocks is not limited
to the fixed size as in the embodiments described above.
For example, the size can be made variable in accordance
20 with setting of the control register or with designation
of the mode signal. When the simultaneous erase voltage
is applied to the word line as being the minimum unit,
for example, the operation of the driver for driving the
word line by the erase voltage may be selected in
25 accordance with setting of the control register or with
the designation of the mode signal.

Further, the mode of division of the memory
block may be such that an entire block is first divided

1 into a plurality of large blocks, and then each of the
large blocks is divided into a plurality of small blocks
so that simultaneous erase can be made in the unit of
the large block or small block.

5 In the system which rewrites the flash memory
under the control of the CPU, a software for self tuning
the rewrite conditions, etc, can also be employed.

In each memory cell transistor of the flash
memory, the source and the drain are relatively
10 recognized in accordance with voltages applied thereto.

The present invention can widely be applied
to, other than a microcomputer, a data processing
apparatus having at least a central processing unit and
an electrically erasable and rewritable nonvolatile
15 flash memory on a single semiconductor chip.